

Claims

- [c1] 1. A method of detecting an interconnection structure having a region within a first wiring level wherein a second layer is not covering a first layer, comprising:
providing the first layer having the second layer on a surface of the first layer; and
creating a recess in the first layer in the region where the second layer is not covering the first layer.
- [c2] 2. The method of claim 1, wherein the recess is created by selectively etching the first layer in the region where the second layer is not covering the first layer.
- [c3] 3. The method of claim 2, wherein at least one of a group of conditions of the selective etch are altered to change a depth of the recess, wherein the group of conditions is selected from a group consisting of: etching material, temperature, power, pressure, and duration of the process.
- [c4] 4. The method of claim 2, wherein the selective etch is performed by a reducing plasma preclean process.
- [c5] 5. The method of claim 4, wherein the reducing plasma preclean process uses a plasma selected from the group consisting of: H_2 , N_2 , NH_3 and noble gases.
- [c6] 6. The method of claim 1, wherein the first layer comprises a

dielectric material selected from a group consisting of: a SiLKTM semiconductor dielectric resin, Teflon, bezocyclobutane-BCB, parylene-N, parylene-F, SiCOH, porous SiO₂, silica aerogels, and FlareTM.

[c7] 7. The method of claim 1, wherein the second layer comprises a hardmask selected from a group consisting of: SiN_x, SiO_xN_y, SiC_x, SiO_xC_y, SiC_xN_y, SiO₂, and SiC_xO_yH_z.

[c8] 8. The method of claim 1, wherein the first layer comprises a material that etches selectively to the second layer with a selectivity of greater than 1 to 1.

[c9] 9. The method of claim 1, after creating a recess in the first layer, further comprising:
forming a plurality of conductive features within a second wiring level of the structure.

[c10] 10. The method of claim 9, wherein the conductive features comprise:
a liner comprising a material selected from the group consisting of: tantalum-based materials, tungsten-based materials and titanium-based materials; and
a conductive material selected from the group consisting of: copper, gold, platinum and silver.

[c11] 11. The method of claim 9, wherein an electrical short between conductive features results if the recess in the first

wiring level replicates in the second wiring level, wherein conductive features are selected from a group consisting of: wires, vias, and wires and vias.

[c12] 12. The method of claim 11, further comprising:
rejecting the interconnection structure if the recess replicates in the second wiring level.

[c13] 13. A structure comprising:
a first wiring level of the structure comprising:
a first layer covering a surface of the structure;
a second layer substantially covering a surface of the first layer; and
a recess formed in a region of the structure where the second layer does not cover the first layer; and
a second wiring level of the structure comprising:
a third layer having a replicated recess in the third layer in the region of the structure where the second layer does not cover the first layer.

[c14] 14. The structure of claim 13, wherein the first layer comprises a dielectric material selected from a group consisting of: a SiLKTM semiconductor dielectric resin, Teflon, bezocyclobutane-BCB, parylene-N, parylene-F, SiCOH, porous SiO₂, silica aerogels, and FlareTM.

[c15] 15. The structure of claim 13, wherein the second layer

comprises a hardmask selected from a group consisting of:
 SiN_x , SiO_xN_y , SiC_x , SiO_xC_y , SiC_xN_y , SiO_2 , and $\text{SiC}_x\text{O}_y\text{H}_z$.

[c16] 16. The structure of claim 13, wherein the replicated recess in the third layer in the region of the structure where the second layer does not cover the first layer produces an electrical short between conductive features within the third layer, wherein the conductive features are selected from a group consisting of: wires, vias, and wires and vias.

[c17] A method of forming an interconnection structure, comprising: using recessed topography formed within a first layer of the structure to indicate the absence of a hardmask covering the first layer.

[c18] 18. The method of claim 17, wherein using the recessed topography within the first layer comprises:
etching the first layer of the structure in a region where the hardmask is not covering the first layer; and
the first layer unetched in a region where the hardmask covers the first layer.

[c19] 19. The method of claim 18, wherein etching the first layer of the structure employs a reducing plasma preclean process.

[c20] The method of claim 19, wherein the reducing plasma preclean process etches the first layer selectively to the hardmask.